A silicon radio-frequency single electron transistor

S. J. Angus,[a] A. J. Ferguson,[b] A. S. Dzurak, and R. G. Clark
Australian Research Council Centre of Excellence for Quantum Computer Technology, The University of New South Wales, Sydney, New South Wales 2052, Australia

(Received 6 September 2007; accepted 14 December 2007; published online 17 March 2008)

We report the demonstration of a silicon radio-frequency single electron transistor. The island is defined by electrostatically tunable tunnel barriers in a narrow channel field effect transistor. Charge sensitivities of better than 10 $\mu e/\sqrt{\text{Hz}}$ are demonstrated at megahertz bandwidth. These results demonstrate that silicon may be used to fabricate fast, sensitive electrometers. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2831664]

Sensitive electrometry allows the electrical properties of quantum dots to be determined without the requirement for electrical transport through the dot itself. In this way, experiments may be performed on a system isolated from electrical contacts. This is particularly desirable for quantum computation where it is interesting to study the coherence of an isolated electron spin,[1] or pair of spins.[2,3] Furthermore, dynamic charge sensing, made possible with the application of radio frequency reflectometry,[4] has resulted in charge detection with greater than megahertz bandwidth.[5–9]

In particular, recent progress in silicon quantum dots calls for the incorporation of a high bandwidth, high sensitivity electrometer to facilitate experiments down to single electron occupancy.[10–12] One possible approach is to utilize an aluminum radio-frequency single electron transistor (rf-SET), however an alternative approach of an integrated silicon rf-SET has the significant benefit of fabrication simplicity. In addition, silicon devices have the potential for larger charging energies than aluminum, leading to increased charge sensitivities as well as higher operating temperatures.[13] In this paper, we demonstrate a silicon rf-SET with a charge sensitivity of better than 10 $\mu e/\sqrt{\text{Hz}}$, at megahertz bandwidth. The SET utilizes a double layer of gates, which enables tuning of the barrier resistances.[12,14] This geometry is related to a GaAs rf-SET,[7] where the charge sensor is located within the semiconductor substrate.

The upper metal-oxide-semiconductor field-effect transistor (MOSFET) gate induces an electron accumulation layer in the high resistivity silicon wafer. The lower gates create tunnel barriers by locally depleting this accumulation layer. This geometry allows the electrostatic creation of small, well-defined dots in silicon.[12] The lower barrier gates are typically less than 30 nm wide, separated by a distance, $d<40$ nm. The width of the upper MOSFET gate of the device reported here was 100 nm.

Electrical transport measurements were performed at the base temperature (~100 mK) of a dilution refrigerator. As illustrated in Fig. 1(c), the silicon SET was placed in an rf tank circuit. A surface-mount inductor $L=470$ nH was used. The capacitance C_P is the parasitic capacitance of the SET to ground. This was determined to be 430–470 fF based on the measurement of the resonant frequency. A dc source-drain bias was applied using a bias tee and two-terminal dc conductance measurements were performed using a standard low-frequency lock-in technique. An rf carrier signal was applied to the source of the SET at the resonant frequency of the circuit (~340 MHz) and the amplified reflected signal was then homodyne detected.

A network analyzer was used to measure the frequency dependence of the reflected rf signal as a function of gate voltage. The reflected signal is described by the reflection coefficient, $r=|(Z-50)/(Z+50)|$, where Z is the impedance of the tank circuit. At the resonant frequency $Z \sim L/(R \times C_P)$, and the reflected rf signal is at a minimum. A change in the resonant frequency f_0 is observed during the gate sweep, shown in Fig. 2(b), which is equivalent to a change in parasitic capacitance of $\Delta C_P=40$ fF. This change in capacitance agrees reasonably well with the capacitance of the induced two-dimensional electron gas (2DEG), estimated using a parallel plate capacitor model, $C_{2\text{DEG}}=20$ fF.[15] The increase in capacitance occurs at an applied gate voltage below the threshold voltage of the device; consistent with the expectation that the wide area leads are induced before the onset of conduction, which is limited by the narrow restriction (100 nm) of the MOSFET channel.[16]

The conductance characteristic of one of the barrier gates is given in Fig. 2(c). The lower gates may be used to tune their associated barrier from highly transparent ($G>e^2/h$) to completely opaque ($G=0$), as illustrated for barrier 2 in Fig. 2(c). Barrier 1 displayed similar conductance and frequency characteristics. There is no significant shift in

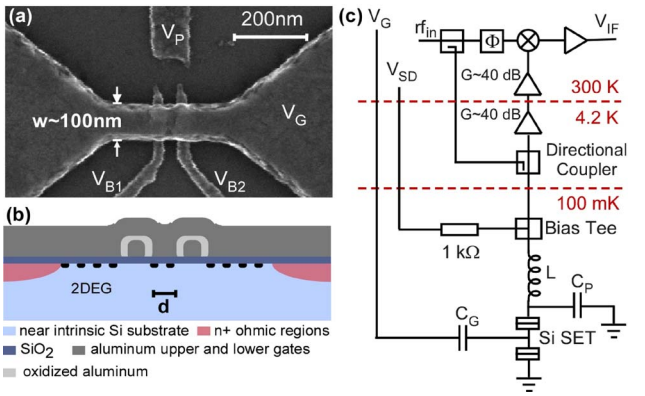

FIG. 1. (Color online) Device structure. (a) Scanning electron micrograph of a typical device. The lower barrier gates, V_{B1} and V_{B2}, are typically <30 nm wide with a separation $d<40$ nm. The width of the upper MOSFET gate V_G is 100 nm. The gate V_P was not used in the experiments reported here. (b) Schematic cross section of a device, illustrating the 2DEG induced in the high resistivity silicon by the upper MOSFET gate, and locally depleted by the lower barrier gates. (c) Schematic of the rf-measurement setup ($L=470$ nH, $C_P=430-470$ fF).

[a]Electronic mail: sjangus@unimelb.edu.au.
[b]Present address: Cavendish Laboratory, University of Cambridge, J.J. Thomson Avenue, Cambridge, CB3 0HE, United Kingdom.

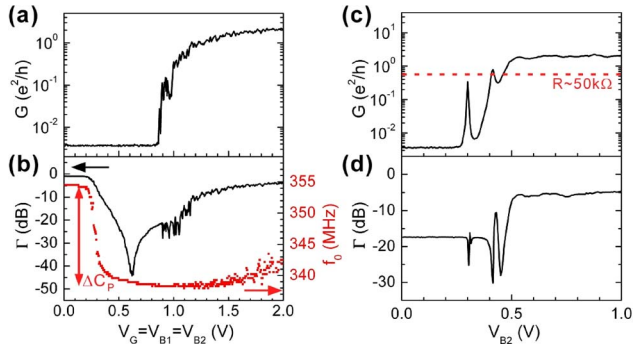

FIG. 2. (Color online) Conductance and reflected power characteristics at $T \sim 100$ mK. The reflected power Γ has not been fully calibrated. Conductance measurements were performed using a standard lock-in technique. The small but finite dc conductance below threshold is an artifact of the measurement set-up. (a) dc conductance as a function of the voltage applied to all gates simultaneously. (b) Reflected rf signal (black) at $f=339$ MHz and measured resonant frequency (red online) as a function of the voltage applied to all gates simultaneously. (c) dc conductance as a function of the voltage applied to one of the barrier gates, V_{B2}. ($V_G=V_{B1}=2.0$ V) (d) Reflected rf signal at $f=338$ MHz as a function of the voltage applied to one of the barrier gates, V_{B2}. ($V_G=V_{B1}=2.0$ V).

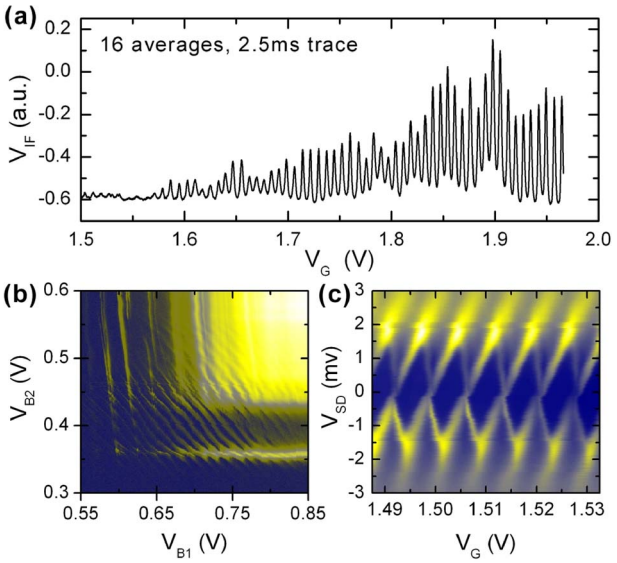

FIG. 3. (Color online) Reflected power measurements demonstrating Coulomb blockade in the silicon SET. An rf carrier signal of 337 MHz was used in (a) and (b) and 334 MHz was used in (c). (a) Reflected power V_{IF} as a function of upper MOSFET gate V_G at $V_{B1}=0.702$ V, $V_{B2}=0.478$ V, and $V_{SD}=0$ mV. (b) Reflected power as a function of both barrier gates, V_{B1} and V_{B2} at $V_G=1.65$ V and $V_{SD}=1.0$ mV, respectively. Blue (grayscale dark) is high reflected power (high resistance), yellow (grayscale light) is low reflected power (low resistance). (c) Coulomb diamonds: reflected power as a function of source-drain bias V_{SD} and upper MOSFET gate bias V_G at $V_{B1}=0.686$ V, $V_{B2}=0.438$ V. Again, blue (grayscale dark) is high reflected power (high resistance), yellow (grayscale light) is low reflected power (low resistance).

resonant frequency during the sweeps of each of the barrier gates.

A comparison of the dc conductance and the reflected rf signal reveals a number of unusual features. Given the inductance ($L=470$ nH) and the capacitance of the circuit ($C_P=470$ fF), the matching resistance is estimated to be 20 kΩ. However, the observed matching resistance appears to be greater than 8 MΩ according to the dc resistance of all gates applied together [Figs. 2(a) and 2(b)], and closer to the expected value ($\sim$50 kΩ) according to the one barrier data in Figs. 2(c) and 2(d). This may be explained by a difference between the dc and the rf conductances of the 2DEG. Previous experimental studies have shown that the conductance of a disordered silicon 2DEG is frequency dependent; at low carrier densities, the conductance increases with frequency, until a maximum conductance is reached at finite frequency.[17] Near the threshold of the sample [below $V_G=V_{B1}=V_{B2}=1.0$ V in Figs. 2(a) and 2(b)], we, therefore, expect greater conductance at radiofrequency than dc. This results in matching being observed while the sample has a high dc resistance. In the one barrier case, however, the density of the 2DEG is high, resulting in closer agreement between the measured dc resistance and the expected resistance at matching.

The Coulomb blockade oscillations are observed over a large range of applied upper MOSFET gate bias V_G while the barrier gates are held at constant potential, as shown in Fig. 2(c). The regular period is evidence that a single dot is formed in the Si SET. We chose to operate the SET near $V_G=1.9$ V due to the large difference in reflected power between the peak and trough of the Coulomb blockade oscillations.

The independent control of each barrier is demonstrated in Fig. 3(b). The vertical and horizontal edges of the conducting region demonstrate that each barrier is able to restrict conduction. The diagonal lines are Coulomb blockade oscillations exhibiting equal coupling to both barriers, indicating regions of constant occupancy in the central island. The vertical (horizontal) lines result from blockade which couples only to V_{B1} (V_{B2}), providing evidence of disorder in each barrier.

Closed, periodic Coulomb diamonds are observed, as shown in Fig. 3(c). The total capacitance of the island may be estimated using a parallel plate capacitor model, resulting in a charging energy of $E_C=2$ meV.[18] This estimate is larger than the charging energy, $E_C=e^2/C_\Sigma \sim 1$ meV, measured at a relatively high applied MOSFET gate bias ($V_G=1.5$ V). This is consistent with previous measurements performed on a similar sample over a large range of applied gate potential, which revealed a decrease in the charging energy with increasing applied upper MOSFET voltage.[12] A higher level of charge noise was observed in this sample, during both dc and rf measurements, than in previous devices. This was not quantified but we attribute this to a strongly coupled fluctuator, possibly located at the silicon-silicon dioxide interface, at a nearby dopant or in one of the barriers.

The charge sensitivity of the silicon rf-SET was determined as a function of carrier frequency, carrier power, gate frequency, and source-drain voltage. A small sinusoidal signal, with an rms amplitude (Δq_{rms}) equivalent to $\sim$0.01 of an electron on the island is superimposed onto the dc gate voltage, producing amplitude modulation of the carrier signal. The charge sensitivity δq is then calculated from the resulting signal to noise ratio of the side-bands according to the expression

$$\delta q = \frac{\Delta q_{\mathrm{rms}}}{\sqrt{2B} \times 10^{\mathrm{SNR}/20}},$$

where B is the resolution bandwidth of the spectrum analyzer and SNR is the signal to noise ratio.[19] The best charge sensitivity was found to be $\delta q=7.2\ \mu e/\sqrt{\mathrm{Hz}}$, at zero source-drain bias.

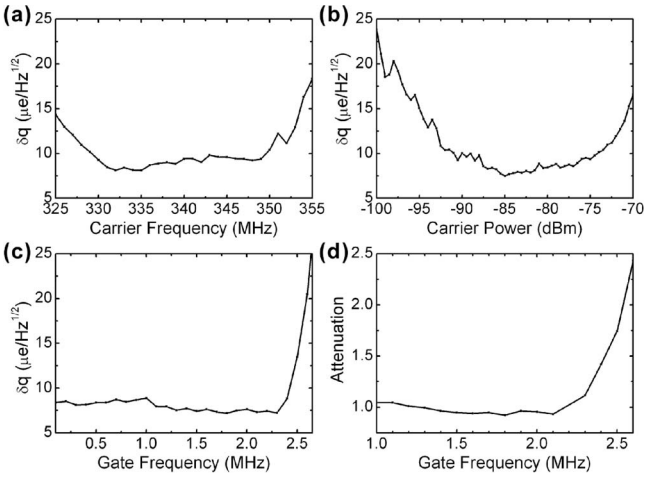

FIG. 4. Charge sensitivity δq at $V_G=1.8625$ V, $V_{B1}=0.716$ V, $V_{B2}=0.438$ V, and $V_{SD}=0$ mV as a function of (a) carrier frequency, (b) carrier power, and (c) gate frequency. (d) Attenuation (linear scale) of the applied gate signal as a function of gate frequency.

The 3 dB bandwidth of the resonant circuit is 20 MHz, as revealed by the dependence of the charge sensitivity on the frequency of the carrier signal, given in Fig. 4(a). This is consistent with the 15 MHz 3 dB resonant bandwidth measured using the network analyzer.

The optimal power of the rf carrier signal, resulting in the largest signal to noise ratio, depends on the charging energy of the SET.[20] We estimate the optimal rf voltage across the SET to have a maximum amplitude $V_{SET} \sim E_C/e$. This voltage is proportional to the incident rf signal V_{rf} by the quality factor of the resonant circuit $Q=\sqrt{L/C_P}/Z_0$ such that $V_{SET}=2QV_{rf}$.[20] In this circuit $Q=20$ resulting in an optimal rf carrier signal $V_{rf} \sim E_c/2Qe=25$ μV (−82 dBm), in good agreement with the measured optimal power of −80–85 dBm, as illustrated in Fig. 4(b).

A sharp deterioration of the charge sensitivity is observed in Fig. 4(c) at an applied gate frequency of approximately 2.5 MHz. This cutoff frequency is consistent with the expected *RC* time constant of the high resistance gate contact in this particular sample.[21] This is confirmed by increasing the amplitude of the sinusoidal signal on the gate across a range of frequencies. Since the SET conductance as a function of gate voltage can be approximated by a sinusoid, as the gate amplitude increases additional sidebands are visible beside the carrier. The magnitude of the *n*th sideband is proportional to the *n*th order Bessel function, $J_n[(2\pi C_G V_G)/e]$. The zeroes of the first sideband reveal the attenuation of the gate signal as a function of frequency, given in Fig. 4(d). The gate signal attenuation rapidly increases at the same gate frequency that the charge sensitivity begins to deteriorate. The apparent drop in sensitivity is, therefore, a result of the reduction in signal reaching the gate.

Possible improvements to the Si rf-SET include increasing the charging energy, leading to both greater charge sensitivity as well as higher maximum operating temperatures. This can be achieved by decreasing the total capacitance, either by decreasing the upper MOSFET gate width, or by increasing the gate oxide thickness. Previous Si SETs made using the same technique as described here have had charging energies up to 4 meV.[12] We note that in this architecture charge detected by the rf-SET will also be coupled to the surface gates, reducing the magnitude of the signal to the rf-SET. This effect can be reduced by increasing the gate oxide thickness.

In conclusion, we have measured a silicon rf-SET fabricated using tunable tunnel barriers in a silicon MOSFET. Charge sensitivity measurements have been reported, demonstrating sensitivities of better than 10 μeV at a bandwidth of 2 MHz, comparable to that of the mature Al rf-SET technology. We look forward to single electron charge sensing in silicon nanostructures using integrated silicon rf-SETs.

The authors thank T. Duty and N. A. Court for helpful discussions and D. Barber and R. P. Starrett for technical support. This work is supported by the Australian Research Council, the Australian Government, and by the US National Security Agency (NSA) and US Army Research Office (ARO) under Contract No. W911NF-04-1-0290.

[1] J. M. Elzerman, R. Hanson, L. H. W. van Beveren, B. Witkamp, L. M. K. Vandersypen, and L. P. Kouwenhoven, Nature (London) **430**, 431 (2004).
[2] F. H. L. Koppens, C. Buizert, K. J. Tielrooij, I. T. Vink, K. C. Nowack, T. Meunier, L. P. Kouwenhoven, and L. M. K. Vandersypen, Nature (London) **442**, 766 (2006).
[3] J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard, Science **309**, 2180 (2005).
[4] R. J. Schoelkopf, P. Wahlgren, A. A. Kozhevnikov, P. Delsing, and D. E. Prober, Science **280**, 1238 (1998).
[5] A. Aassime, G. Johansson, G. Wendin, R. J. Schoelkopf, and P. Delsing, Phys. Rev. Lett. **86**, 3376 (2001).
[6] W. Lu, Z. Q. Ji, L. Pfeiffer, K. W. West, and A. J. Rimberg, Nature (London) **423**, 422 (2003).
[7] T. Fujisawa, T. Hayashi, Y. Hirayama, H. D. Cheong, and Y. H. Jeong, Appl. Phys. Lett. **84**, 2343 (2004).
[8] M. J. Biercuk, D. J. Reilly, T. M. Buehler, V. C. Chan, J. M. Chow, R. G. Clark, and C. M. Marcus, Phys. Rev. B **73**, 201402 (2006).
[9] T. M. Buehler, V. Chan, A. J. Ferguson, A. S. Dzurak, F. E. Hudson, D. J. Reilly, A. R. Hamilton, R. G. Clark, D. N. Jamieson, C. Yang, C. I. Pakes, and S. Prawer, Appl. Phys. Lett. **88**, 192101 (2006).
[10] H. W. Liu, T. Fujisawa, Y. Ono, H. Inokawa, A. Fujiwara, K. Takashina, and Y. Hirayama, e-print arXiv:0707.3513v1 (2007).
[11] L. J. Klein, D. E. Savage, and M. A. Eriksson, Appl. Phys. Lett. **90**, 033103 (2007).
[12] S. J. Angus, A. J. Ferguson, A. S. Dzurak, and R. G. Clark, Nano Lett. **7**, 2051 (2007).
[13] Y. Ono, A. Fujiwara, K. Nishiguchi, H. Inokawa, and Y. Takahashi, J. Appl. Phys. **97**, 031101 (2005).
[14] A. Fujiwara, H. Inokawa, K. Yamazaki, H. Namatsu, Y. Takahashi, N. M. Zimmerman, and S. B. Martin, Appl. Phys. Lett. **88**, 053121 (2006).
[15] The capacitance of the induced 2DEG is estimated using $C_{2DEG}=(\epsilon_r\epsilon_0\Delta A)/d=20$ fF, where the area of the 2DEG $\Delta A=3$ μm^2, the relative dielectric constant of the silicon dioxide $\epsilon_r=3.9$ and the oxide thickness $d=5$ nm.
[16] A. T. Tilke, F. C. Simmel, H. Lorenz, R. H. Blick, and J. P. Kotthaus, Phys. Rev. B **68**, 075311 (2003).
[17] A. Gold, S. J. Allen, B. A. Wilson, and D. C. Tsui, Phys. Rev. B **25**, 3519 (1982).
[18] The total capacitance of the island is estimated according to $C_\Sigma=(\epsilon_0\epsilon_r A)/d=70$ aF, where the relative dielectric constant of SiO_2 $\epsilon_r=3.9$, $A=100\times100$ nm^2 (including the capacitance of the dot to the barrier gates as well as to the upper gate) and the thickness of the oxide, $d=5$ nm.
[19] L. Roschier, P. Hakonen, K. Bladh, P. Delsing, K. W. Lehnert, L. Spietz, and R. J. Schoelkopf, J. Appl. Phys. **95**, 1274 (2004).
[20] A. N. Korotkov and M. A. Paalanen, Appl. Phys. Lett. **74**, 4052 (1999).
[21] The EBL defined aluminum gate connects to a larger area aluminum bond pad. This contact has an area of approximately 4×6 μm^2, a resistance of ~1 MΩ and a capacitance estimated to be 500 fF (assuming a parallel plate capacitor with a dielectric constant of the Al_2O_3 of 7). The high resistance of the gate contact is due to contacting two layers of aluminum, without removing the native aluminum oxide between them. This results in a *RC* time constant of 500 ns, and a cutoff frequency of 2 MHz.