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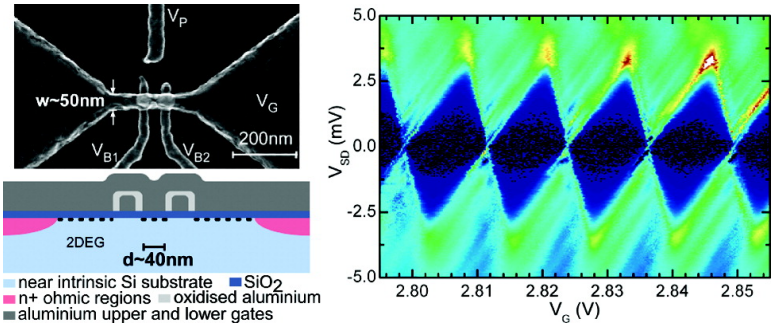

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Gate-Defined Quantum Dots in Intrinsic Silicon

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ABSTRACT

We report the fabrication and measurement of silicon quantum dots with tunable tunnel barriers in a narrow-channel field-effect transistor. Low-temperature transport spectroscopy is performed in both the many-electron (∼100 electrons) regime and the few-electron (∼10 electrons) regime. Excited states in the bias spectroscopy provide evidence of quantum confinement. These results demonstrate that depletion gates are an effective technique for defining quantum dots in silicon.

All electrically measured single-electron devices and quantum dots require tunnel barriers. These barriers fall into two broad categories: those in which the transparency is fixed during fabrication, and those where the transparency can be tuned in situ between opaque and highly conducting. Tunable tunnel barriers are particularly desirable in quantum dots, where it is often necessary to control the tunnel rate across a barrier, or to manage the interaction between electron occupancy and barrier transparency. Recent achievements in controlling and measuring spin in GaAs-based semiconductor quantum dots[1−3] have been substantially facilitated by a tunable gate architecture. Electrostatically tunable barriers have also been used to create well-defined quantum dots in other low-dimensional systems (for example, semiconducting carbon nanotubes[4,5] and InAs nanowires[6]).

Silicon is a particularly attractive material for use to investigate quantum dots, because of the expected long electron-spin coherence time. This is a result of the small spin−orbit coupling in silicon and the primarily spin-zero nuclear background.[7] However, single-electron spins have not yet been investigated in silicon quantum dots.

Recently, there has been considerable progress toward this goal. Coulomb blockade has been observed in etched Si/SiGe heterostructures,[8] and, more recently, quantum dots have been defined in Si/SiGe using a Schottky split-gate technique.[9−12] Fixed tunnel barriers, such as local dopant modulation[13] or etching,[14,15] have been used to fabricate quantum dots in silicon-on-insulator material. Silicon nanowires have also been shown to confine a quantum dot, with the source and drain contacts forming the tunnel barriers.[16] Electrostatic tunnel barriers have been created using various double-gated structures.[17,18] In a structure related to that reported in this paper, polysilicon gates have been used to define a single- and double-island single-electron transistor (SET) electrostatically.[19] Significantly, however, a reproducible technique to produce quantum confined dots with tunable barriers in silicon has not been demonstrated previously.

In this paper, we report transport measurements of quantum dots created by tunable barriers in a silicon narrow-channel field-effect transistor. Partial oxidation of a lower layer of aluminum barrier gates creates a very thin, localized layer of aluminum oxide, which enables the deposition of an isolated top gate. This technique, which is based on a native aluminum oxide, has not previously been utilized in silicon devices. This geometry allows the electrostatic creation of small, well-defined dots in silicon with a diameter of ∼50 nm, resulting in quantum confinement, as evidenced by excited-state bias spectroscopy. We have measured several devices and report here on two such dots.

High resistivity (>10 kΩ/cm^2) near-intrinsic silicon wafers[20] were used, with phosphorus-diffused regions as ohmic contacts. A 5-nm-thick SiO_2 gate oxide was thermally grown on the surface. The lower aluminum barrier gates were fabricated using electron-beam lithography (EBL), thermal evaporation, and liftoff. These gates were then partially oxidized using a plasma oxidation technique. The aluminum gates were exposed to a low-pressure oxygen plasma (0.15 mbar) for 3 min at a temperature of ∼150 °C. This causes the aluminum to form a layer of aluminum oxide (a few nanometers thick) at the surface.[21] Many test samples were fabricated for the purpose of breakdown tests, which confirmed that the partial oxidation of the lower layer sufficiently insulates it from the upper layer of aluminum.[22] A similar process has been used previously in multilayer aluminum SETs[23] and also carbon nanotube devices.[24] The upper aluminum gate was aligned to the lower gates during

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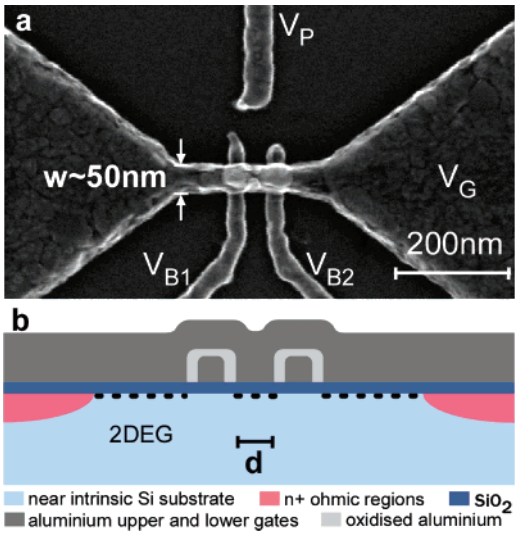

Figure 1. Device structure. (a) Scanning electron microscopy (SEM) micrograph of a typical device. The lower barrier gates, V_{B1} and V_{B2}, are typically <30 nm wide with a separation of d < 40 nm. The widths of the upper MOSFET gates (V_G) of the two devices reported here were $w = 60$ and 100 nm. The plunger gate (V_P) was not used in the experiments reported here. (b) Schematic cross section of a device, illustrating the 2DEG induced in the high resistivity silicon by the upper MOSFET gate and locally depleted by the lower barrier gates.

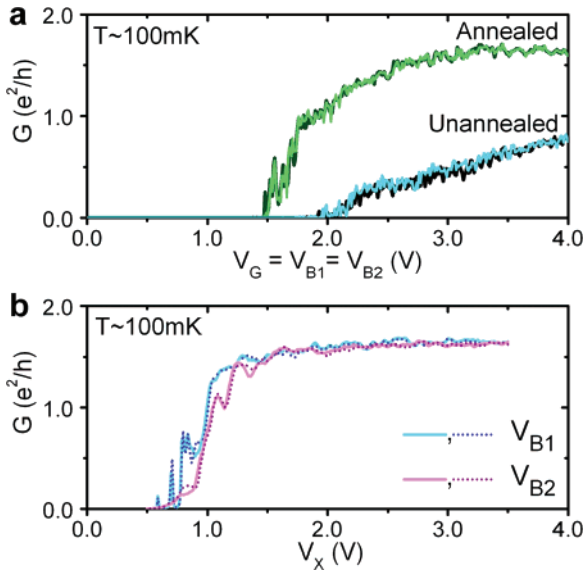

Figure 2. Two-terminal conductance characteristics of sample 1 at $T \approx 100$ mK, measured using a lock-in AC excitation voltage of 100 μV. Each ohmic contact typically has a resistance of ~1 kΩ. The typical maximum mobility of similar MOSFET devices (5-nm SiO_2, Al gate) is ~5000 $cm^2/(V\ s)$ at 4 K. (a) Comparison of the turn-on characteristic of annealed and unannealed devices; the annealed devices have a reduced threshold voltage, increased transconductance, and an increased maximum conductance, and the fluctuations in the annealed devices are reproducible. (b) The conductance response of each barrier gate, measured while the upper MOSFET gate and the other barrier gate were well above the threshold value ($V_G = V_{BY} = 3.5$ V). The barriers both have a steeper turn-on than the MOSFET channel. Some resonances can be observed in each barrier.

a second EBL stage, and again thermally evaporated and lifted off. The final step of processing was a low-temperature-forming gas anneal (15 min at 400 °C in 95% N_2/5% H_2). A scanning electron microscopy (SEM) image of a device is provided in Figure 1, along with a schematic cross section. The lower barrier gates are typically <30 nm wide, separated by a distance d of <40 nm. The widths of the upper gates of the two devices reported here were 60 nm and 100 nm.

Electrical transport measurements were performed on several silicon quantum dots at the base temperature (~50 mK) of a dilution refrigerator, at an electron temperature of ~100 mK. Standard low-frequency lock-in techniques were used to measure the two-terminal conductance and differential conductance through the dot. Measurements were performed in zero applied magnetic field.

To measure the turn-on characteristic, a voltage was applied to all three gates simultaneously, resulting in an approximately continuous field along the length of the nanowire. At 4 K, because of the high resistivity of the wafer, the source-drain conductance is zero until the applied gate voltage is equal to the threshold value. As the applied gate voltage is increased above the threshold value, the source-drain current increases smoothly toward a maximum conductance. At millikelvin temperatures, conductance fluctuations occur in the MOSFET turn-on characteristic. As shown in Figure 2, these fluctuations are reproducible over several sweeps. These fluctuations may result from Coulomb blockade in the MOSFET channel or universal conductance fluctuations; further experiments are needed to confirm their origin. This is in contrast to devices made in the same batch, but without the final forming gas anneal. The fluctuations in these samples were not reproducible over different sweeps and were time-dependent, which is consistent with switching events at the unannealed Si/SiO_2 interface or within the SiO_2. A forming gas anneal is well-established in standard Si MOSFETs for reducing the Si/SiO_2 interface trap density, and we emphasize the importance of this step for noise reduction in low-temperature measurements. This anneal also improved the performance of our samples by decreasing the threshold voltage, increasing the transconductance, and increasing the maximum conductance. Each of these effects is visible in the comparison of the annealed and unannealed samples in Figure 2a.

The conductance characteristic of each of the barrier gates is shown in Figure 2b. To isolate the effect of each barrier gate, these characteristics were measured with both the upper MOSFET gate and the other respective barrier gate well above the threshold value. These results demonstrate that each of the lower gates may be used to tune its associated barrier from highly transparent ($G > e^2/h$) to completely opaque ($G = 0$). Some conductance fluctuations are observed in each barrier, which are probably due to variations in the potential and resonances in each barrier. At 4 K, these fluctuations are not observed; the source-drain conductance increases smoothly with the applied barrier gate voltage.

The combined effect of both the upper MOSFET gate and the lower barrier gates on the source-drain conductance is illustrated in Figure 3. The constant period and varying amplitude of the Coulomb oscillations, as shown in Figure 3a, are typical of transport through a semiconducting island.

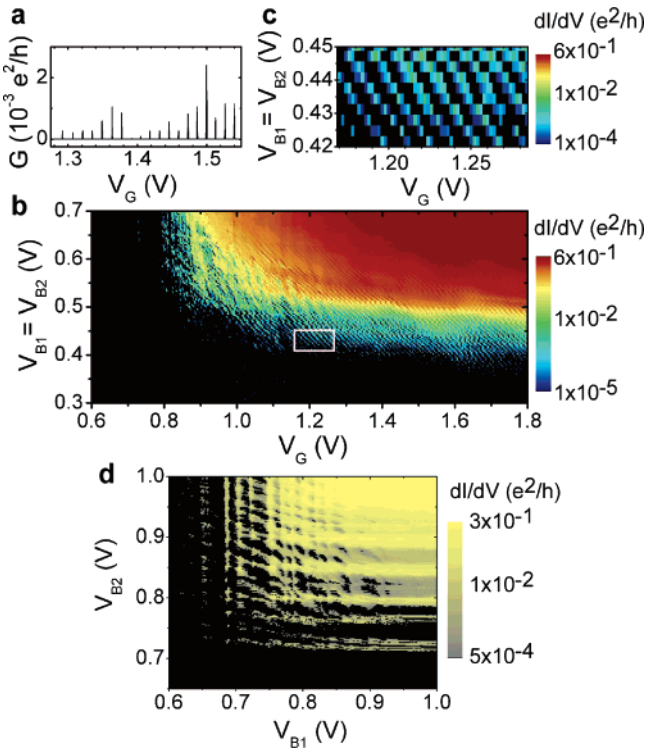

Figure 3. Characterization of sample 2 (during two thermal cycles). A lock-in AC excitation of 50 μV was used. (a) Single trace at V_{B1} = 0.43 V, V_{B2} = 0.37 V, showing the Coulomb blockade oscillations. (Thermal cycle 2.) (b) Differential conductance as a function of the upper MOSFET gate (V_G) and the barrier gates (V_{B1} and V_{B2}). A constant source-drain bias of 1.5 mV was applied. (Thermal cycle 2.) (c) Enlarged section of panel b, highlighting the diagonal lines of constant occupancy of the dot; the slope of these lines results from the capacitive coupling of the dot to both the upper MOSFET gate (V_G) and the barrier gates (V_{B1} and V_{B2}). (d) Differential conductance as a function of each barrier gate (V_{B1} and V_{B2}) at V_G = 1.3 V, measured using a constant source-drain bias of 1.5 mV. (Thermal cycle 1.)

Figure 3b displays the relationship between the upper and lower gates. The current through the device is zero when the applied MOSFET gate voltage (V_G) is below the threshold value, and also when opaque barriers are created by the lower gates (V_{B1} or V_{B2}). When the source-drain current through the device is nonzero, Coulomb blockade with constant period is observed over a large region, demonstrating that a single island is formed by the tunable tunnel barriers over a large range of applied biases. The fine diagonal lines in the plot, which are enlarged in Figure 3c to be more easily visible, correspond to regions of constant electron occupancy of the dot.

The independent control of each barrier is demonstrated further in Figure 3d. Diagonal lines in the plot indicate Coulomb blockade that is equally coupled to each barrier gate and, therefore, is due to the central island. Also visible are vertical and horizontal lines, which are evidence of Coulomb blockade that is strongly coupled to the first and second barrier gates, respectively. The very small cross-coupling shown makes it likely that these resonances are due to the imperfect potential in each of the barriers. Irregularities in the transport through the dot, as observed in Figure 3b,

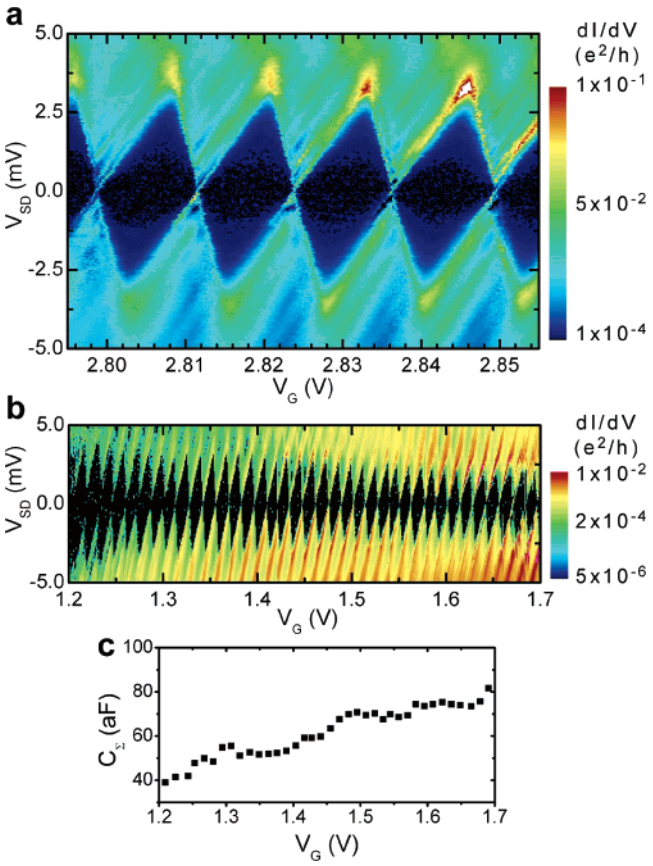

Figure 4. Bias spectroscopy of two different samples, both in the many-electron regime: (a) sample 1, taken at $V_{B1} = V_{B2} = 0.85$ V, with a lock-in AC excitation voltage of 20 μV, $N \approx 100$ electrons; (b) sample 2 (thermal cycle 2), taken at $V_{B1} = 0.43$ V, $V_{B2} = 0.37$ V, with a lock-in AC excitation voltage of 50 μV, $N \approx 30$ electrons on the left; (c) total capacitance of sample 2, as a function of the applied MOSFET gate voltage (V_G).

are likely to result from this same disorder in the barriers. We note that, in Figure 3d, there is some capacitive coupling between these barrier resonances and the central island, which may be suggestive of double dot charging. However, when the upper MOSFET gate (V_G) is used to probe the Coulomb diamonds, a constant Coulomb blockade period is observed over a wide range (for example, see Figure 4b). This is indicative of a single dot in the centrally defined island.

Various devices have been measured, with consistent results across different samples. Figure 4 shows Coulomb diamonds belonging to two different samples: sample 1 in Figure 4a (with a dot area of 30 nm $\times$ 105 nm), and sample 2 in Figure 4b (dot area = 35 nm $\times$ 65 nm). The dot in sample 1 has a charging energy of $e^2/C_\Sigma = 2.5$ meV. This gives a total capacitance value for the defined quantum dot of 64 aF, which is consistent with a simple parallel plate capacitance calculation of 61 aF, based on the lithographic dimensions of the dot, including the contribution of the barrier gates. The gate capacitance (determined by the period of oscillations) is determined to be 13 aF, which, again, is consistent with the parallel-plate capacitor estimation of 21 aF. The ratio of the gate capacitance to the total capacitance is $\alpha = C_G/C_\Sigma = 0.20$.

The dot in sample 2 (Figure 4b) has a charging energy, e^2/C_Σ, which increases from 2 meV to 4 meV, as the applied MOSFET gate voltage, V_G, decreases. This charging energy is larger, which is consistent with the smaller dimensions of this device. The total capacitance determined from the charging energy is 40−80 aF, and this finding again agrees with the calculated capacitance of 41 aF. The total capacitance is approximately linearly dependent on the applied MOSFET gate voltage V_G, as shown in Figure 4c, because the capacitance increases as the size of the dot increases. The gate capacitance is determined to be 12 aF, from the period of oscillations, which is consistent with the calculated value of 16 aF. The gate capacitance does not change significantly over the applied voltage range, presumably because, as the dot extends under the barrier gates, it is electrostatically screened from the applied MOSFET gate voltage. This results in a gate capacitance ratio of $\alpha = 0.30$ at $V_G = 1.2$ V. The consistency of regular diamonds over such a large gate range confirms that this sample contains a single, electrostatically defined quantum dot, because multiple islands result in overlapping diamonds.[25]

By varying the voltages applied to the upper gate and the lower gates, it is possible to measure transport through the quantum dot in different regimes: the upper MOSFET gate (V_G) is used to alter the number of electrons in the dot; and the lower barriers gates control the coupling between the dot and the leads. We chose to investigate the few-electron regime and also the many-electron regime in a weakly coupled dot.

Both bias spectroscopy plots shown in Figure 4 were taken in the many-electron regime. We estimated the number of electrons in the dot using two different methods. The first method used the period of Coulomb oscillations, which represents the addition of a single electron. The relative voltage applied to the top gate, with respect to the threshold voltage, is divided by the Coulomb oscillation period, giving an estimate of the number of electrons in the dot (assuming zero free electrons in the dot below the threshold voltage). The second method simply used the measured electron density of a similar MOSFET device.[26] Both methods give consistent estimates, within a few electrons. The number of electrons (N) in each of the dots shown is thus estimated to be $N \approx 100$ in Figure 4a and $N \approx 30$ at the left of the long diamond sweep in Figure 4b.

To investigate transport phenomena in the few-electron regime, the applied MOSFET gate bias V_G was reduced to just above the threshold value. Figure 5 shows data obtained with $V_G = 1.10$ V, where we estimate $N \approx 10$ electrons.

There are indications of excited states (shown in Figure 5 by brighter lines of differential conductance parallel to the edges of the Coulomb diamonds outside of the blockaded region) in the many-electron regime; however, these states become far more pronounced in the few-electron regime, as observed in Figure 5b in particular. The approximate energy level spacing in a two-dimensional (2D) dot can be calculated using

$$\Delta E = \frac{2\pi\hbar^2}{gm^*A}$$

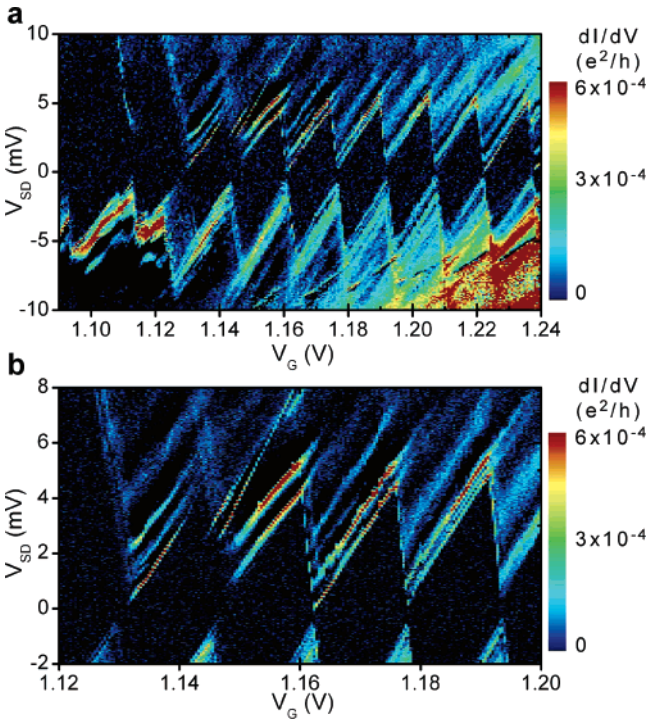

Figure 5. Bias spectroscopy of sample 2, taken in the few-electron regime, during thermal cycle 1, where a lock-in excitation of 50 μV was used: (a) the number of electrons were reduced by decreasing the voltage applied to the MOSFET top gate (the Coulomb diamonds shown here were the last visible, taken at $V_{B1} = V_{B2} = 0.754$ V); (b) the lines of conductance parallel to the Coulomb diamond edges in this enlarged view are evidence of excited states in the device. These diamonds were again taken at $V_{B1} = V_{B2} = 0.754$ V.

where g is the degeneracy, m^* the effective mass, and A the area of the dot.[25] If both spin and valley degeneracies are included, then $\Delta E = 275$ μeV. Energy-level spacings up to 600 μeV are observed in Figure 5, which is broadly consistent with the predicted value. In the few-electron regime, there are also many anomalies in the Coulomb diamonds, such as the gap in conductance near $V_{SD} = 0$ mV and also the brighter lines of conductance that are not parallel to the diamonds. We understand that these are mostly likely due to imperfections in the barriers.

Detailed quantitative analysis of the excited-state energy levels is not included in this paper, although it is interesting to note several features. Significantly, the spacing of the excited states changes considerably for different electron occupancy of the dot, which is consistent with the excited states of a dot in the few-electron regime. States in the barriers or leads are expected to remain at a constant spacing over several diamonds. It is not clear whether the excited states of the dot are due to orbital excited states alone or whether there is also a splitting of the 2D valley degeneracy, as is anticipated in strongly confined 2D structures in silicon.[27]

Recently, progress in GaAs quantum dots has advanced significantly because of optimization of surface gate geometry, in particular, enabling measurements to be performed on lateral quantum dots occupied by a single electron. Results reported here are significant motivation for similar work to

be performed in regard to optimizing surface gates in silicon. There are many parameters in the simple fabrication of these devices that may be adjusted to optimize the dot characteristics. Reduced barrier width may remove some of the resonances observed in Figure 3. Reduced dot size should decrease the number of electrons in the dot at a given electron density, as well as increase the energy scales. Increased SiO_2 thickness may smooth variations in applied gate potentials.

In conclusion, we have described a simple new technique that enables the fabrication of single quantum dots with tunable barriers in bulk silicon. Transport measurements of two different dots have been reported, with bias spectroscopy performed in both the many-electron and few-electron regimes. Evidence of excited states in these dots has been shown, demonstrating their quantum confinement. The tunable barriers of these dots enable further investigation of many fundamental properties of silicon quantum dots, such as the Kondo effect and spin and valley degeneracies. The quantum confinement shown also leads to an anticipation that single-spin manipulation and measurement, which, so far, has been only realized in GaAs, may also be realized in silicon quantum dots.

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References

(1) Elzerman, J. M.; Hanson, R.; Willems van Beveren, L. H.; Witkamp, B.; K. Vandersypen, L. M.; Kouwenhoven, L. P. *Nature* **2004**, *430*, 431.
(2) Petta, J. R.; Johnson, A. C.; Taylor, J. M.; Laird, E. A.; Yacoby, A.; Lukin, M. D.; Marcus, C. M.; Hanson, M. P.; Gossard, A. C. *Science* **2005**, *309*, 2180.
(3) Koppens, F. H. L.; Buizert, C.; Tielrooij, K. J.; Vink, I. T.; Nowack, K. C.; Meunier, T.; Kouwenhoven, L. P.; Vandersypen, L. M. K. *Nature* **2006**, *442*, 766.
(4) Biercuk, M. J.; Mason, N.; Marcus, C. M. *Nano Lett.* **2004**, *4*, 1.
(5) Sapmaz, S.; Meyer, C.; Beliczynski, P.; Jarillo-Herrero, P.; Kouwenhoven, L. P. *Nano Lett.* **2006**, *6*, 1350.
(6) Fasth, C.; Fuhrer, A.; Bjork, M. T.; Samuelson, L. *Nano Lett.* **2005**, *5*, 1487.
(7) Tahan, C.; Joynt, R. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2005**, *71*, 075315.
(8) Klein, L. J.; Lewis, K. L. M.; Slinker, K. A.; Goswami, S.; van der Weide, D. W.; Blick, R. H.; Mooney, P. M.; Chu, J. O.; Coppersmith, S. N.; Friesen, M.; Eriksson, M. A. *J. Appl. Phys.* **2006**, *99*, 023509.
(9) Berer, T.; Pachinger, D.; Pillwein, G.; Muhlberger, M.; Lichtenberger, H.; Brunthaler, G.; Schaffler, F. *Appl. Phys. Lett.* **2006**, *88*, 162112.
(10) Sakr, M. R.; Jiang, H. W.; Yablonovitch, E.; Croke, E. T. *Appl. Phys. Lett.* **2005**, *87*, 223104.
(11) Klein, L. J.; Savage, D. E.; Eriksson, M. A. *Appl. Phys. Lett.* **2007**, *90*, 033103.
(12) Goswami, S.; Slinker, K. A.; Friesen, M.; McGuire, L. M.; Truitt, J. L.; Tahan, C.; Klein, L. J.; Chu, J. O.; Mooney, P. M.; van der Weide, D. W.; Joynt, R.; Coppersmith, S. N.; Eriksson, M. A. *Nat. Phys.* **2007**, *3*, 41.
(13) Hofheinz, M.; Jehl, X.; Sanquer, M.; Molas, G.; Vinet, M.; Deleonibus, S. *Appl. Phys. Lett.* **2006**, *89*, 143504.
(14) Rokhinson, L. P.; Guo, L. J.; Chou, S. Y.; Tsui, D. C. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2001**, *63*, 035321.
(15) Saitoh, M.; Saito, T.; Inukai, T.; Hiramoto, T. *Appl. Phys. Lett.* **2001**, *79*, 2025.
(16) Zhong, Z. H.; Fang, Y.; Lu, W.; Lieber, C. M. *Nano Lett.* **2005**, *5*, 1143.
(17) Simmel, F.; Abusch-Magder, D.; Wharam, D. A.; Kastner, M. A.; Kotthaus, J. P. *Phys. Rev. B: Condens. Matter Mater. Phys.* **1999**, *59*, 10441.
(18) Jones, G. M.; Hu, B. H.; Yang, C. H.; Yang, M. J.; Hajdaj, R.; Hehein, G. *Appl. Phys. Lett.* **2006**, *89*, 073106.
(19) Fujiwara, A.; Inokawa, H.; Yamazaki, K.; Namatsu, H.; Takahashi, Y.; Zimmerman, N. M.; Martin, S. B. *Appl. Phys. Lett.* **2006**, *88*, 053121.
(20) Topsil HPS wafers were used, which have a weak residual *n*-type (phosphorus) doping ($<10^{12}$ cm^{-3}).
(21) Heij, C. P. Ph.D. Thesis, Delft University of Technology, Delft, The Netherlands, 2001.
(22) The test samples consisted of two aluminium electrodes, overlapping in a 1 μm $\times$ 1 μm region, insulated according to the AlO*x* technique described. The voltage required to cause breakdown of the AlO*x* was measured for each sample. The minimum breakdown voltage measured was 2.5 V. Approximately half of the samples (11/20) had a breakdown voltage between 2.5 V and 3.5 V, and the remainder (9/20) broke down at >3.5 V. This demonstrates that the native AlO*x* provides sufficient insulation up to at least 2.5 V. In fact, the quantum dot devices measured have consistently sustained a 3.0 V difference across the layers without breakdown, perhaps because of their much smaller overlap area (30 nm $\times$ 50 nm).
(23) Heij, C. P.; Hadley, P.; Mooij, J. E. *Appl. Phys. Lett.* **2001**, *78*, 1140.
(24) Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. *Science* **2001**, *294*, 1317.
(25) Sohn, L. L., Kouwenhoven, L. P., Schoen, G., Eds. *Mesoscopic Electron Transport*; NATO ASI Series E; Kluwer Academic Publishers: Dordrecht, The Netherlands, 1997.
(26) Hall measurements have been performed on larger Hall-bar MOSFETs (5 nm SiO_2, Al gate) by D. R. McCamey. The relationship between the carrier density (n) and the applied voltage (V_G) was determined to be $n = 3.5 \times (V_G - V_T)\ 10^{12}$ cm^{-2}, where V_T is the threshold voltage.
(27) Ando, T.; Fowler, A. B.; Stern, F. *Rev. Mod. Phys.* **1982**, *54*, 437.

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