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Tunable aluminium-gated single electron transistor on a doped silicon-on-insulator etched nanowire

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We report the fabrication and electrical characterization of an electrostatically defined aluminum-gated SET on a lightly doped SOI etched nanowire based on MOSFET structures. The tunability of the device is achieved via two sets of electrically isolated aluminum surface gates. The results demonstrate a reproducible constant charging energy of 2 meV for a large range of gate voltages as well as tunable tunneling resistance. The controllable tunnel barriers permit transport spectroscopy of subthreshhold features. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4750251]

Single electron transistors (SETs) are one of the building blocks of quantum information processing due to the possibility to use them as a ultrasensitive electrometers.[1–3] Recently, the interaction between artificial atoms and single dopants impurities has been investigated as possible hybrid systems for quantum computing.[4,5] A number of groups have demonstrated the reproducible fabrication of SETs on Si and Ge nanowires.[6–8] This 3D technology shows several advantages over standard planar fabrication techniques[9] such as reduced source drain leakage currents and good control over the central islands size and, therefore, the charging energy. This could allow operation at higher temperatures[10,11] or improve the sensitivity of the SET as a charge sensor. Moreover, the etched nanowire technology provides an excellent platform to study single dopant effects. The reduced size limits the total number of dopants and reduces the dipolar interaction with surrounding impurities.[12] Furthermore, the dopants are located close to the active region of the device enhancing its capacitive coupling.[13,14] To study dopants, a full control over the tunnel barriers is desirable,[15] unlike devices where the shape of the tunnel barriers are defined by the doping profile[6] or etched constrictions.[16] The operation of Si-SETs with flexible control of the tunnel barriers has been electrostatically achieved via polycrystalline silicon tunnel barrier gates.[17] In such devices unintentional floating gates formed in the polycrystalline silicon gates contribute additional charge noise.[18]

In this letter, we report the fabrication and electrical characterization of a silicon SET on lithographically silicon-on-insulator (SOI) nanowires implanted with a low dose of arsenic dopants. In contrast to earlier studies, our design makes use of aluminum gates to form the tunnel barriers, which should provide a reliable platform for dopant studies. We discuss the device fabrication, followed by a presentation of electrical measurements of Coulomb blockade (CB) oscillations and the investigation of subthreshhold features.

The device fabrication starts with a 100 nm-thick (100)-oriented p-type SOI wafer with an electrical resistivity of 13–22 Ωcm and a 200 nm-thick buried oxide layer (BOX). Prior to ion implantation, an 18 nm sacrificial oxide is thermally grown to protect from implantation damage. Source and drain ohmic regions separated by 2 μm are implanted with phosphorus (Dose = 10^{15} cm^{-2}, E = 22 keV). A second ultra low-dose global arsenic implant is performed (Dose = 2×10^{10}cm^{-2}, E = 90 keV). The nanowire structure and local alignment markers are defined by electron beam lithography (EBL) and 50 nm aluminum thermal evaporation, serving as an etch mask. The pattern is transferred via reactive ion etching (CF_4 in 20% O_2) down to the BOX. After metal and sacrificial oxide removal, a high quality 18 nm gate oxide is grown at 850 °C for 55 min followed by a 20 min argon anneal at 950 °C to reduce the fixed oxide charge density.[19] The resulting wire is 25 nm wide, 85 nm high, and 1 μm long. The 150 nm wide barrier gates (SB and DB) are defined using EBL, followed by 120 nm thermal aluminum evaporation and lift off. These gates are partially oxidized at 150 °C for 5 min[20] to form a 4 nm-thick AlO_x layer to electrically isolate them from a topgate, which is fabricated using EBL and 150 nm thermal aluminum evaporation. It completely covers the wire and overlaps with the doped source and drain regions. Finally, a low-temperature forming gas anneal (15 min at 400 °C in N_2/H_2 5%) was executed to reduce the density of interface trap charges.[21] A cross section schematic of the device as well as scanning electron microscope image is shown in Figs. 1(a) and 1(b). The dimensions of the central island are lithographically defined by the separation of the aluminum tunnel barriers (90 nm) and the width of the Si wire (25 nm).

The devices have been characterized by two terminal DC transport as well as low-frequency lock-in measurements. In Fig. 1(c), the conductivity of the device is plotted as a function of the voltage applied simultaneously to all three gates for a temperature of 300 K and 290 mK. At room temperature, the device behaves like a metal-oxide-semiconductor field effect transistor (MOSFET) with a threshold voltage of 0.1 V. At 290 mK, the structure presents conductance oscillations close to turn-on (V = 1.4 V), which arise from the nonuniformity of the 2DEG. Well above threshold (V > 2 V), the 2DEG is well defined across the nanowire and the oscillations disappear. The data presented in the following are recorded with $V_{tg} = 3$ V.

In some cases, the barrier gates show highly resistive discontinuities where they wrap around the wire. Bond pads

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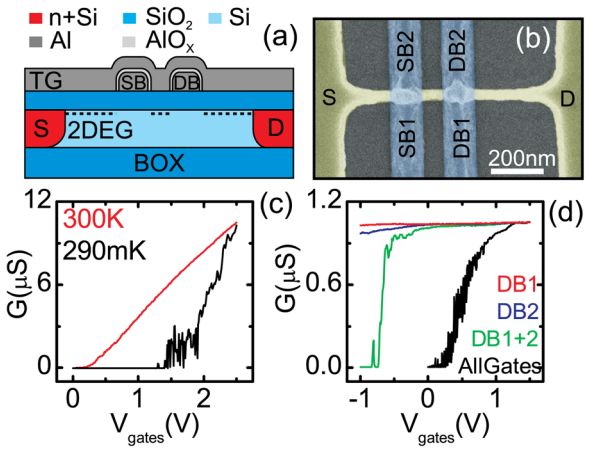

FIG. 1. Device structure and characterization. (a) Schematic cross section of the device indicating the accumulation of a 2DEG at the Si/SiO_2 interface and the local depletion by the barrier gates. (b) Scanning electron microscopy top-view of the device before the top gate is deposited. (c) Turn-on characteristics of the device at 300 K and 290 mK when a positive voltage is applied to all the three surface gates. $V_{sd} = 1$ mV. (d) Data from a different device at 4.2 K. Drain barrier gate presents an electrical discontinuity. Dual-side gating (DB1 and DB2 simultaneously biased) allows flexible control of the tunnel barrier.

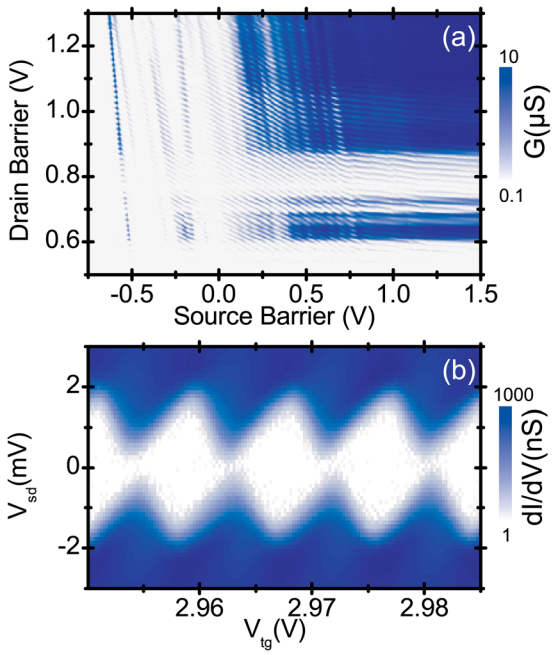

FIG. 2. SET characterization at 290 mK. (a) Device conductance as a function of the barrier gate voltages for $V_{tg} = 3$ V and $V_{sd} = 1$ mV. (b) Coulomb blockade diamonds as a function of V_{tg} for $V_{bs} = 230$ mV and $V_{bd} = 900$ mV. Differential conductance measured using a lock-in excitation voltage of 200 μeV.

connected to the barrier gates have been added on both sides of the structure to measure the resistance of the barrier gate crossing the wire. Of 15 barrier gates tested, 5 presented a low resistance of 10 Ω at 4.2 K, while 10 showed electrical discontinuity. Depositing the metal gates with sputter coating could provide more uniform coverage on the sidewalls of the wire than thermal evaporation. Additionally, the difference in thermal expansion coefficients for aluminum (23.1×10^{-6}m/K) and silicon (2.6×10^{-6}m/K)[22] must be considered, since the fabrication and measurement process involves a temperature range from cryogenic temperatures up to 400 °C. Gate metals with a lower thermal expansion coefficients like titanium (8.6×10^{-6}m/K) or tungsten (4.5×10^{-6}m/K)[22] might be more suitable.

We tested the tunability of the barriers by measuring the source drain current with $V_{tg} = V_{bs} = 1.5$ V as a function of the drain barrier gate voltages V_{bd1} and V_{bd2} on a different device. The measurement is presented in Fig. 1(d). For single sided gating (DB1 or DB2), the reduction of the current is less than 10%. Dual sided gating (DB1 + DB2), on the other hand, allows complete tunability of the tunnel barrier from fully transparent to opaque.

The CB operation of the SET can be characterized by independently sweeping the voltage on the source and drain barrier gates (V_{bd}, V_{bs}) and monitoring the source drain current, which is presented in Fig. 2(a) for $V_{sd} = 1$ mV at T = 290 mK. A well-defined SET island equally coupled to both barriers can be identified by diagonal lines of increased current in the plot. This regime spans from $V_{bd} = 0.6$ to 1.2 V and $V_{bs} = 0$ to 0.75 V in our measurement. Such a large range of SET operation is of extreme importance in studies of dopants coupled to a charge sensing device. Additionally, vertical and horizontal lines indicate the presence of CB oscillations strongly coupled to each barrier. These oscillations can originate from Coulomb blockade in the disordered potential underneath the wide barriers[9] or resonant tunneling through dopant states.[23]

In Fig. 2(b), we present the differential conductance of the device as a function of V_{sd} and V_{tg} for $V_{bs} = 230$ mV and $V_{bd} = 900$ mV. Coulomb diamonds are observed over several charge transitions with a charging energy of $E_c = e^2/2C_\Sigma = 2.1 \pm 0.2$ meV. The period of the oscillations is $\Delta V_{tg} = 8.7$ mV, from which we estimate an electron number of 170 on the island, a gate capacitance of $C_{tg} = e/\Delta V_{tg} = 18.5$ aF, and a lever arm $\alpha = C_{tg}/C_\Sigma = 0.24$. This value is consistent with an elliptical capacitor model where we calculate $C_{tg} = \pi\epsilon_{ox} L/\ln(\frac{d_{Si}}{2} + h_{Si} + 2t_{ox}/\frac{d_{Si}}{2} + h_{Si}) = 30$ aF. Here, d_{Si} (h_{Si}) is the width (height) of the Si core and t_{ox} is the oxide thickness. The values have been assigned according to the lithographic dimensions of the device. The source and drain capacitances $C_s = 30 \pm 6$ aF and $C_d = 28 \pm 6$ aF are extracted from the slopes of the Coulomb diamonds. This indicates that the charge island is equally coupled to the leads and well centered. The capacitances found from further devices showed a variation of less than 25%, exemplifying the reproducibility of the fabrication process.

We now focus on the electrical tunability of the device. Fig. 3(a) shows a large V_{tg} scan where regular CB oscillations can be observed over a range of top gate voltages. No satellite transitions are present in the stability diagram indicating the formation of a well-defined charge island and no unintentional floating islands in the gates. The absence of switching events indicates the quality of the interface with a low density of interface traps. The total capacitance of the device, presented in Fig. 3(b), increases slightly as V_{tg} increases. This is consistent with a increased area as the central island penetrates more into the barrier gate area at higher V_{tg}. On the other hand, CB oscillations are presented in Figs. 3(c)–3(e) for a range of barrier gates voltages exemplifying the large barrier voltage space in which the SET presents

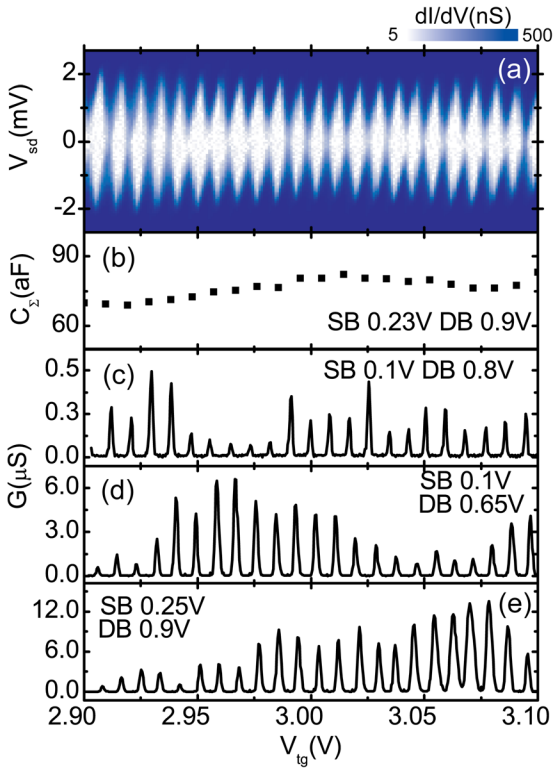

FIG. 3. Device tunability. (a) Stability diagram for a large range of top gate voltages showing periodic regular Coulomb diamonds. Lock-in AC excitation of 200 μeV. $V_{bs} = 230$ mV and $V_{bd} = 900$ mV. (b) Total capacitance of the SET island as a function of V_{tg}. Periodic CB oscillations for different barrier gates biasing conditions for $V_{sd} = 0.1$ mV: (c) $V_{bs} = 100$ mV, $V_{bd} = 800$ mV, (d) $V_{bs} = 100$ mV, $V_{bd} = 650$ mV, (e) $V_{bs} = 250$ mV, $V_{bd} = 900$ mV.

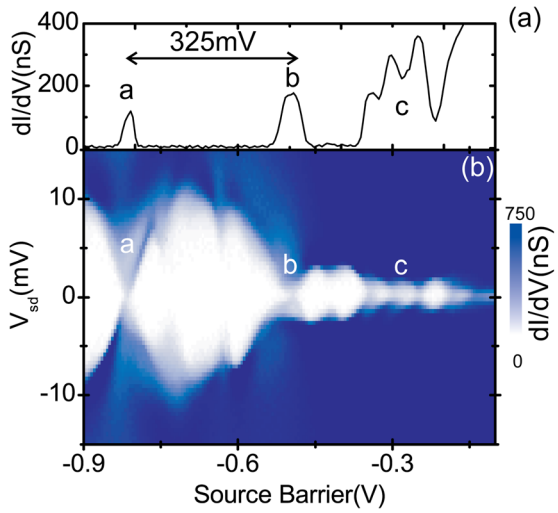

FIG. 4. Dopant signatures. (a) Source barrier voltage differential conductance at low V_{bs}. Two clear transition a, b are observable in the subthreshold regime as well as irregular resonances c at larger V_{bs}. (b) Source barrier stability diagram acquired with a lock-in AC excitation voltage of 200 μeV. The charging energy of the system is 20 meV.

Coulomb blockade. The different conductance scales in Figs. 3(c)–3(e) indicate that the tunneling resistances of the barriers can be modified from several megaohms to just below 100 kΩ. This low resistance limit makes this structures ideal for radiofrequency impedance matching achieved by embedding the SET in a reflectometry tank circuit.[24] Finally, we discuss the tunability of the sensitivity of the SET as a charge sensor. The intrinsic charge sensitivity of the SET can be calculated from $\delta q = C_{tg}\sqrt{eI}/g_m$, where I is the current through the SET and $g_m = \partial I/\partial V_{tg}$ is the transconductance.[25] From the slope of the peaks in Figs. 3(c)–3(e), we estimate a sensitivity ranging from 5 $\mu e/\sqrt{Hz}$ to 1 $\mu e/\sqrt{Hz}$.

Finally, we discuss the origin of the subthreshold features observed in Fig. 2(a). Such transitions can arise from the formation of unintentional quantum dots or due to transport through impurity states in the doped Si substrate. To obtain further insight, we measured the differential conductance of the source barrier as a function of V_{bs}, which is presented in Fig. 4(a). Above the threshold of the barrier $V_{bs} = -200$ mV, the nanostructure becomes transparent. For $V_{bs} > -400$ mV, several irregular transitions labeled c are observed. At $V_{bs} = -818$ mV and -493 mV, the data show two clear transitions marked a and b, respectively. Below $V_{bs} = -818$ mV, no further conductivity peaks are detected.

Figure 4(b) shows a measurement of the differential conductance of transitions a-c as a function of V_{sd} and V_{bs}. The drain barrier and the top gate were biased at 3 V. The slopes of the conducting sectors provide a measurement of the coupling between the gating electrode and the corresponding charge site, $\alpha = C_{bs}/C_\Sigma$, where C_{bs} is the capacitance between the charge center and the source barrier gate and C_Σ is the total capacitance of the center. For transitions a and b, we extract a lever arm of $\alpha_a = 0.07$ and $\alpha_b = 0.05$, respectively. These values suggest that the resonances come from the same charge site and the small difference arise due to thinner barriers at higher V_{bs}. Using the averaged value of $\alpha = 0.06$, the voltage separation $\Delta V = 325$ mV translates into an energy of $E_c = 19.5$ meV. This result agrees well with previously reported charging energies for dopants situated close to a metal-oxide-semiconductor interface, where E_c is lower than the bulk value of $E_c = 52$ meV[26] due to the electrostatic coupling to the nearby electrodes.[23] This suggests that transitions a and b could arise from the filling sequence of an arsenic dopant in silicon. Moreover, we simulated the arsenic implantation profile to obtain a statistical estimate of the number of dopants expected under the barrier gate volume. For this purpose, we used an implantation Monte-Carlo simulator (SRIM). The results show an averaged density of 2.5×10^{15}cm^{-3} and, therefore, a mean number of dopants of 1 per tunnel barrier. The transitions c, on the other hand, show a much smaller charging energy of $E_c = 1.4$ meV and are energetically much closer to the threshold of the barrier. We interpret these peaks as transport through unintentionally formed quantum dots underneath the source barrier. While these first observations do not allow an unambiguous identification of dopant atoms, they motivate further investigations.

In conclusion, we have demonstrated a tunable aluminum-gated SET on a doped silicon etched nanowire. The breaking of the aluminum tunnel barriers was overcome by double-side gating. The results show reproducible charging energies as well as controllable charge sensitivity. The reproducibility and tunability of these devices combined with a low level of charge noise make this kind of structures good candidates to study the properties of isolated impurity atoms in metal-oxide-semiconductor devices. Finally, we investigated subthreshold features in the tunnel barrier of the SET.

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